User Manual

GHD3440

Three-phase 200V Gate Driver

Version: V1.0

Contents

1 Product overview

1.1 Introduction

GHD3440 is a three-phase medium-voltage high-speed gate drive IC, which is specially designed for driving double-N-channel VDMOS power transistor or IGBT in bridge circuits, and is suitable for application schemes for battery-powered DC brushless motors. The embedded typical dead time is 250ns. When the dead time of the MCU output signal is less than the embedded dead time, the actual dead time is the embedded dead time. On the contrary, when the dead time of the MCU output signal is greater than the embedded dead time, the actual dead time is the output dead time of MCU. The embedded VCC and VBS undervoltage protection functions can prevent the system from turning on the external power transistors at low driving voltage. The output of the high-side driving circuit and the output of the low-side driving circuit are controlled through input signals.

1.2 Product Type and Package

GHD3440 has two package types.

Table 1 Product Type and Package

Product Type	Product Package
GHD3440PF	TSSOP20
GHD3440QE	QFN24

1.3 Main characteristics

- Operating supply voltage range: 5.5~18V
- Floating offset voltage: +200V
- Embedded minimum dead time: 250ns
- Embedded VCC and VBS undervoltage protection
- Embedded straight-through prevention function
- Embedded input pull-down resistor
- Embedded output pull-down resistor
- Matching the transmission time of high and low-end channels
- High dv/dt noise suppression capability
- Input and output in-phase
- Compatible with 3.3V/5V logic input
- Peak input current 1.0A@12V, 3.3nF load fall time 60ns
- Peak output current 0.8A@12V, 3.3nF load rise time 90ns

1.4 Application scope

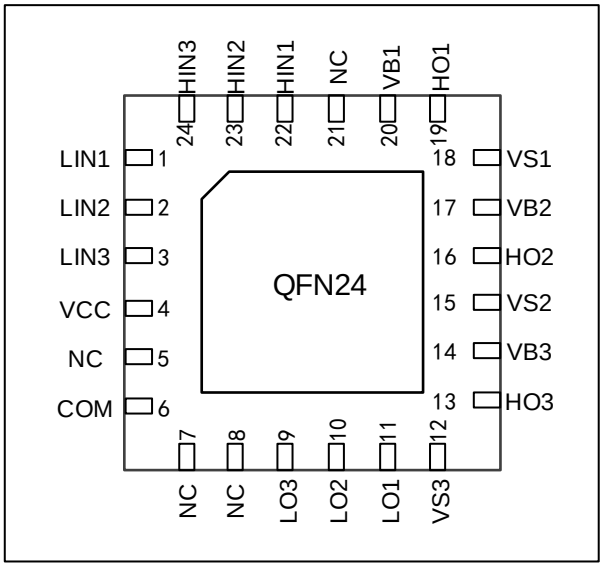
- Various tools based on DC brushless motors in battery-powered systems
- Electric tools, such as electric wrenches, electric screwdrivers, electric drills, and electric hammers
- Garden tools, such as lawn mowers, pruners, hedge trimmers, and chain saws
- Cleaning tools, such as electric cleaning brushes and vacuum cleaners

2 Pin information

2.1 Pin distribution

Figure 1 Distribution Diagram of TSSOP20 Pins

Figure 2 Distribution Diagram of QFN24 Pins



2.2 Pin functional description

Table 2 Legends/Abbreviations Used in Output Pin Table

Name	Abbreviations	Definitions
Pin Name	Unless otherwise specified in the bracket below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type	P	Power supply pin
	I	Only input pin
	I/O	I/O pin

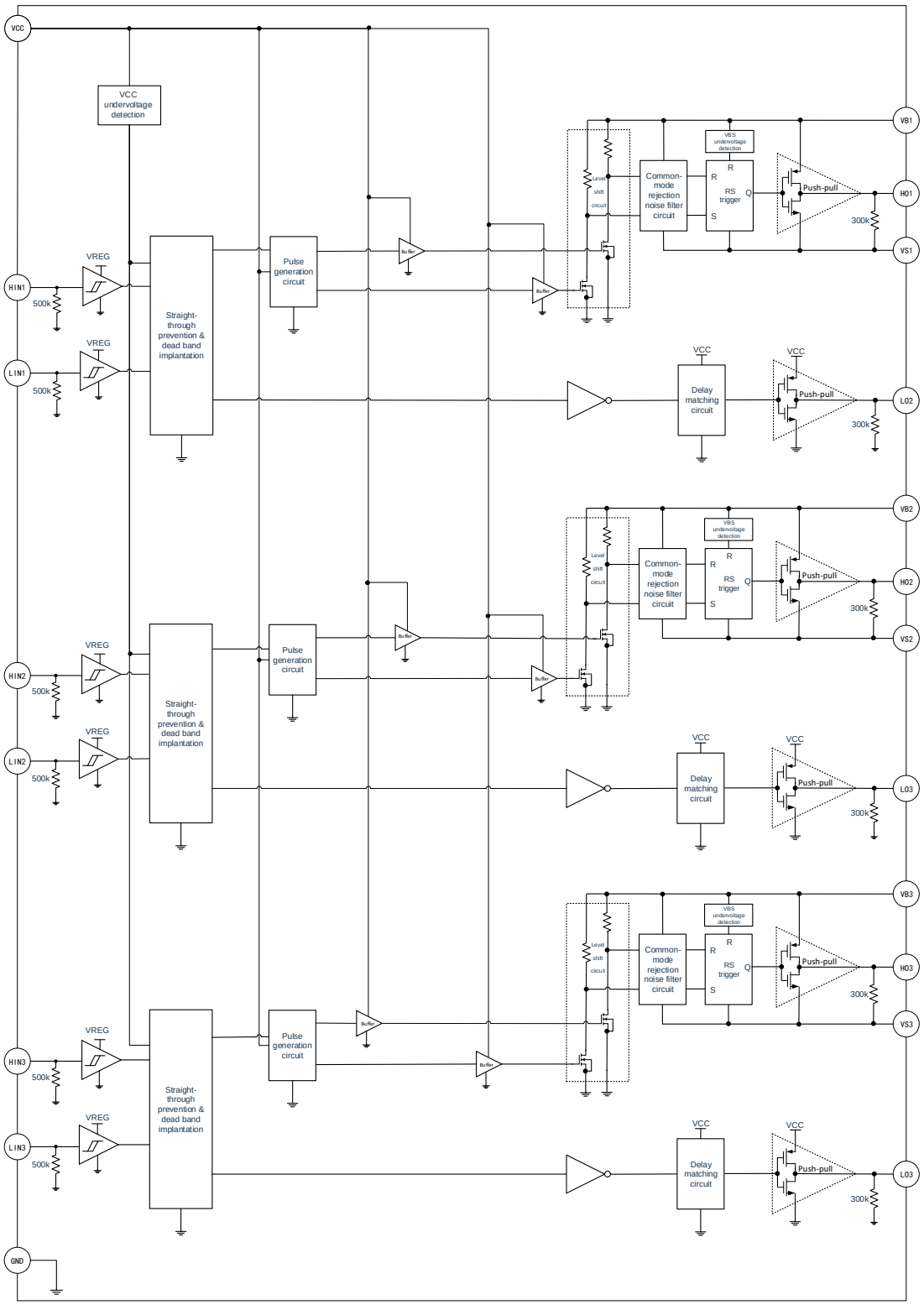
Table 3 Description of GHD3440 by Pin Number

Name	Type	Functional Description	TSSOP20 Pin Sequence	QFN24 Pin Sequence
HIN1	I	Phase-1 high-side input	1	22
HIN2	I	Phase-2 high-side input	2	23
HIN3	I	Phase-3 high-side input	3	24
LIN1	I	Phase-1 low-side input	4	1
LIN2	I	Phase-2 low-side input	5	2
LIN3	I	Phase-3 low-side input	6	3
VCC	P	Power supply	7	4
GND	P	Ground	8	6
LO3	O	Phase-3 low-side output	9	9
LO2	O	Phase-2 low-side output	10	10
LO1	O	Phase-1 low-side output	11	11
VS3	P	Phase-3 high-side floating end	12	12
HO3	O	Phase-3 high-side output	13	13
VB3	P	Phase-3 high-side bootstrap power end	14	14
VS2	P	Phase-2 high-side floating end	15	15
HO2	O	Phase-2 high-side output	16	16
VB2	P	Phase-2 high-side bootstrap power end	17	17
VS1	P	Phase-1 high-side floating end	18	18
HO1	O	Phase-1 high-side output	19	19
VB1	P	Phase-1 high-side bootstrap power end	20	20
NC	-	-	-	5,7,8,21

3 Block diagram logic

3.1 Internal block diagram

Figure 3 GHD3440 Internal Block Diagram



3.2 Logic truth value

Table 4 Logic Truth Value

VCCUV	VBSUV	LIN	HIN	LO	HO
normal	normal	L	H	L	H
		H	L	H	L
		L	L	L	L
		H	H	L	L
under vccuv		L	H	L	L
		H	L	L	L
		L	L	L	L
		H	H	L	L
normal	under vbsuv	L	H	L	L
		H	L	H	L
		L	L	L	L
		H	H	L	L

4 Electrical characteristics

4.1 Recommended safe operating range

T_A=25℃, all pins take GND as the reference points, unless otherwise specified.

Table 5 General Operating Conditions

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
T_A	Ambient temperature	-40	-	105	℃
$V_{HO1,2,3}$	High-side output voltage	$VS_{1,2,3}$	$VS_{1,2,3}$+12	$VB_{1,2,3}$	V
$V_{LO1,2,3}$	Low-side output voltage	0	12	VCC	V
$VB_{1,2,3}$	High-side floating offset absolute voltage	$VS_{1,2,3}$+5	$VS_{1,2,3}$+12	$VS_{1,2,3}$+18	V
$VS_{1,2,3}$	High-side floating offset relative voltage	GND-5	-	140	V
VCC	Supply voltage	5.5	12	18	V
V_{IN}	Input voltage (HIN1, 2, 3/LIN1, 2, 3)	0	-	5	V

Note:

(1) When VB1, 2, 3=VS1, 2, 3+10, and VS1, 2, 3 is (COM-5V)~(COM-VBS), the HO logic state is maintained. When VS1, 2, 3 is (COM-5V)~140V, HO operates normally.

(2) Operation beyond the recommended conditions for a long time may affect its reliability.

4.2 Absolute maximum rated value

T_A=25℃, all pins take GND as the reference points, unless otherwise specified.

Table 6 Power Consumption

Symbol	Description	Minimum value	Maximum value	Unit
P_D	Maximum power consumption	-	1.25	W

Note: At any time, the power consumption cannot exceed P_D. The calculation formula for the maximum power consumption at different ambient temperatures is: $P_D=(150℃-T_A)/\theta_{JA}$, 150℃ is the maximum operating junction temperature of the circuit, T_A is the operating ambient temperature of the circuit, and θ_{JA} is the thermal resistance of the package.

Table 7 Temperature Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
T_s	Storage temperature	-55	150	℃
θ_{JA}	Junction-to-ambient thermal resistance	-	100	℃/W
T_J	Junction temperature	-	150	℃
T_L	Pin welding temperature (duration 10s)	-	260	℃

Table 8 Maximum Rated Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
$V_{HO1,2,3}$	High-side output voltage	$VS_{1,2,3}$-0.3	$VB_{1,2,3}$+0.3	V
$V_{LO1,2,3}$	Low-side output voltage	-0.3	VCC+0.3	V
$VB_{1,2,3}$	High-side floating offset absolute voltage	-0.3	220	V
$VS_{1,2,3}$	High-side floating offset relative voltage	$VB_{1,2,3}$-25	$VB_{1,2,3}$+0.3	V
VCC	Maximum supply voltage	-0.3	20	V
V_{IN}	Maximum input voltage （HIN1,2,3/LIN1,2,3）	-0.7	10	V
dVS/dt	Maximum slew rate of offset voltage	-	50	V/ns

Table 9 ESD Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
$V_{ESD（HBM）}$	Electrostatic discharge voltage (human body model)	-	1000	V

Note: JEDEC document JEP155 states that 1000V HBM can be safely manufactured under standard ESD control procedures.

4.3 Electrical characteristic parameters

T_A=25℃, VCC=$VBS_{1,2,3}$=12V, $VS_{1,2,3}$=GND; all pins take GND as the reference points, unless otherwise specified.

Table 10 Supply Voltage Parameters

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
VBS_{HY+}	VBS undervoltage high-level potential	4.1	4.4	4.9	V
VBS_{HY-}	VBS undervoltage low-level potential	3.8	4.1	4.6	V
VBS_{HY}	VBS undervoltage hysteresis level	0.2	0.3	0.4	V
VCC_{HY+}	VCC undervoltage high-level potential	4.3	4.6	5.1	V
VCC_{HY-}	VCC undervoltage low-level potential	4.0	4.3	4.7	V
VCC_{HY}	VCC undervoltage hysteresis level	0.2	0.3	0.4	V

Table 11 Supply Current Parameters

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
I_{CCD}	VCC dynamic current	$f_{LIN1,2,3}$=20kHz	300	500	800	uA
I_{BSD}	VBS dynamic current	$f_{HIN1,2,3}$=20kHz	120	170	300	uA
I_{CCQ}	VCC static current	V_{IN}=0V	120	165	250	uA
I_{BSQ}	VBS static current	V_{HIN}=0V	35	50	70	uA
I_{LK}	VB floating power supply leakage current	VB=220V	0	0.1	5	uA

Table 12 Time Parameters

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{ON}	Output rising edge transmission time	No Load	160	200	350	ns
t_{OFF}	Output falling edge transmission time	No Load	160	200	350	ns
t_r	Output rise time	C_L=3.3nF	60	90	150	ns
t_f	Output fall time	C_L=3.3nF	40	60	90	ns
DT	Dead time	No Load	200	250	400	ns
MT	High and low-side matching time	No Load	0	30	50	ns

Table 13 Input-end Parameters

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{IN+}	Input high-level potential		1.70	2.15	2.40	V
V_{IN-}	Input low-level potential		0.65	1.45	1.85	V
I_{IN+}	Input high-level current	V_{IN}=5V	8	11	15	uA
I_{IN-}	Input low-level current	V_{IN}=0V	-1	0	1	uA
V_{INHY}	Input hysteresis level		0.45	0.7	1.1	V

Table 14 Outut-end Parameters

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{OUT+}	High-level output voltage	I_{OUT}=100mA 15V- V_{OUT}	0.5	0.64	1.0	V
V_{OUT-}	Low-level output voltage	I_{OUT}=100mA V_{OUT}-GND	0.2	0.28	0.48	V
V_{OUT-}	Low-level output voltage	I_{OUT}=10mA 12V- V_{OUT}	0.05	0.07	0.1	V
V_{OUT-}	Low-level output voltage	I_{OUT}=10mA V_{OUT}-GND	0.02	0.04	0.08	V
I_{OUT+}	High-level short-circuit pulse current	V_{IN}=5V V_O=0V PWD≤10μs	0.60	0.8	1.4	A
I_{OUT-}	Low-level short-circuit pulse current	V_{IN}=0V V_O=15V PWD≤10μs	0.75	1.0	1.75	A

5 Description of application

5.1 Recommended application circuit diagram

Figure 4 Application Circuit

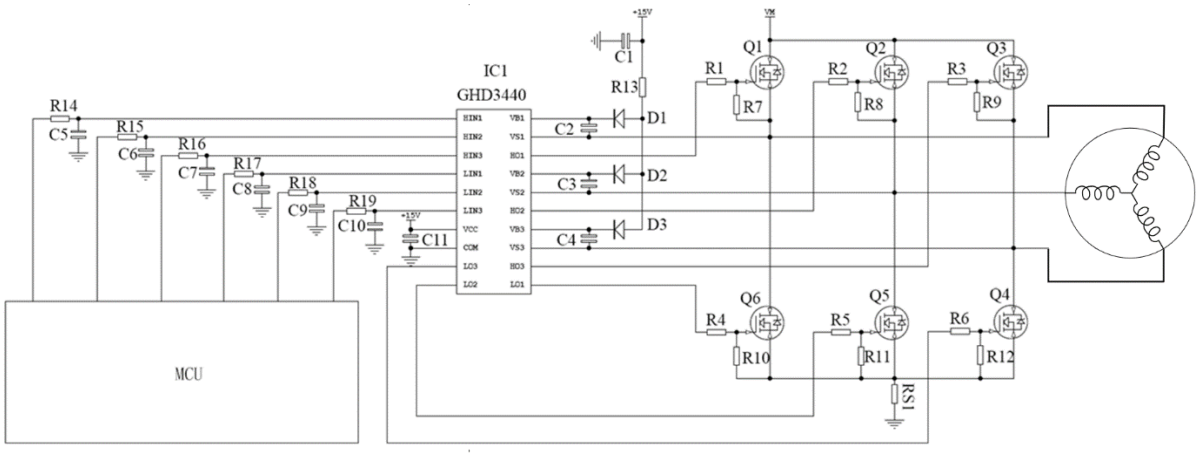
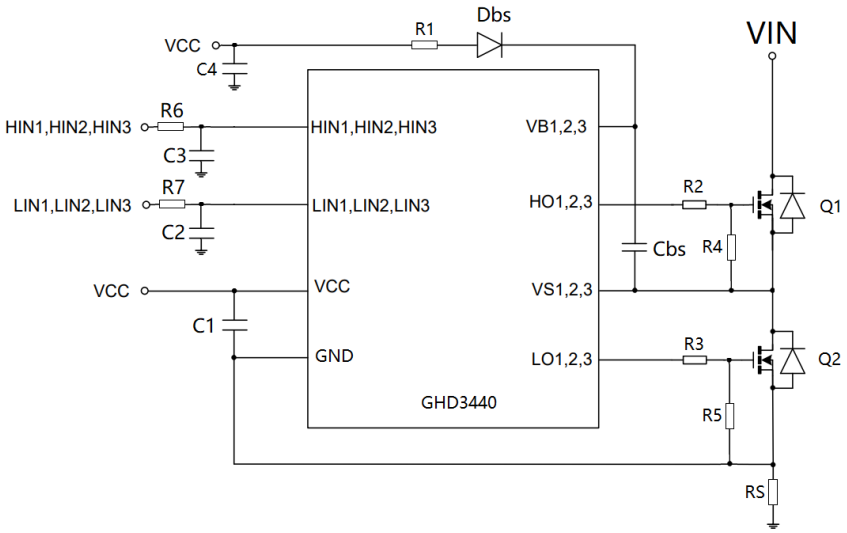


Table 15 Recommended Parameters

Position number	Typical application value	Remarks
C11	10uF/25V/X7R/1206	Select the capacitors with large capacitance values to ensure stable power supply
C1	4.7uF/25V/X7R/1206	Select based on practical application
R14, R15, R16, R17, R18, R19	100Ω/0603	Select based on measured signal waveform in practical application
C5, C6, C7, C8, C9, C10	100pF/X7R/0603	Select based on measured signal waveform in practical application
C2, C3, C4	10uF/25V/X7R/1206	Select based on actual power transistor and switching frequency
R1, R2, R3, R4, R5, R6	10Ω/0603	Select based on actual power transistor and Vgs driving waveform
R7, R8, R9, R10, R11, R12	30KΩ/0603	Determine whether to retain the output bias resistor based on practical application requirements
R13	10Ω/0805	Select based on the bootstrap capacitance value and switching frequency
D1, D2, D3	Determine based on the practical application	Select the diode with a short recovery time according to the practical application and the voltage margin and overcurrent capacity.
Q1, Q2, Q3, Q4, Q5, Q6	Determine based on the practical application	Select according to the practical application and the voltage margin and overcurrent capacity.
RS1	Determine based on the practical application	Select according to the practical application and the errors, temperature drift, and power margin.

5.2 PCB layout suggestions

Figure 5 PCB Layout Schematic Circuit



(1) The chip-powered filter capacitor C1 is placed nearby between the GHD3440 VCC pin and GND pin, and the bootstrap current limiting resistor R1, bootstrap diode Dbs, and bootstrap capacitor Cbs are placed nearby at the corresponding pin of GHD3440 to minimize the circuit area.

(2) Minimize the routing between the MCU PWM output and the GHD3440 PWM input as much as possible, and place the R6, C3, R7, and C2 filter resistors and capacitors close to the GHD3440 pin.

(3) Place the driving gate resistor R2, R3, and gate pull-down resistors R4, R5 close to the Q1 and Q2 gates to reduce the oscillation caused by the routing inductor to the driving signals.

(4) The area of the power circuit should be as small as possible, and the power ground, power ground, and signal ground should be routed separately.

(5) If a DC-DC switching power supply is used in the circuit, the operating frequency of the DC-DC circuit should be high, and the circuit area should be as small as possible. It is best to arrange this part according to the recommended layout for the used DC-DC chip.

5.3 Selection of peripheral devices

(1) The bootstrap capacitor with low ESR is recommended, with a voltage resistance of 2*VCC or above, and a capacitance value within 1u~100uF. It shall be select based on the actual observed ripple, and be used in conjunction with a clamping diode.

(2) The bootstrap diode with fast recovery is recommended, with a voltage resistance of 2*VIN or above and an instantaneous current value greater than 1A. It shall be used in conjunction with a current limiting resistor according to the actual power-on and charging time.

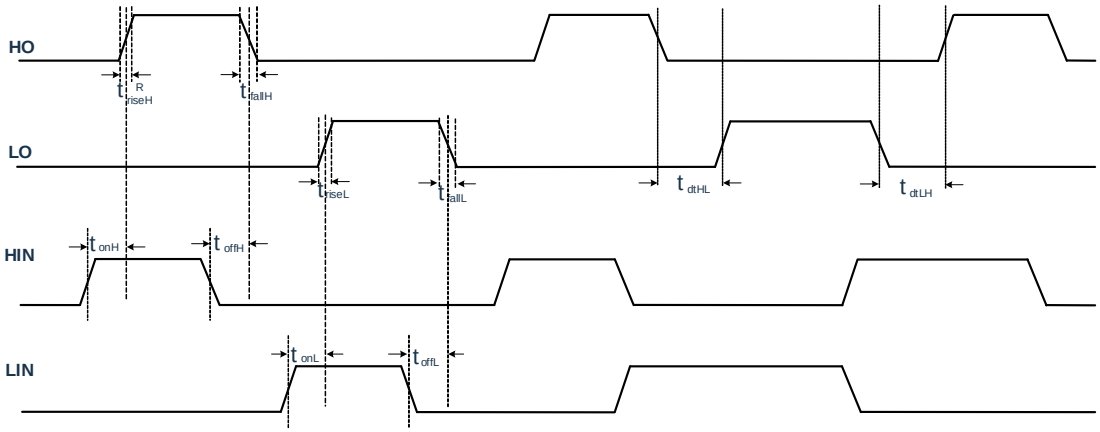
(3) The driving resistance is determined by the parameters of the driven device, dead time, MOSFET power consumption, and electromagnetic compatibility. It is recommended to use the backward diode or PNP triode to quickly turn off the circuit.

6 Test instructions

6.1 Time parameter test

The time parameters mainly include the output rise time t_{rise}, the output fall time t_{fall}, the rising edge transmission time t_{on}, the falling edge transmission time t_{off}, and the dead time t_{dt}.

Figure 6 Time Parameters



6.2 VCC and VBS undervoltage test

VCC and VBS are the power supply ends of low/high circuit, respectively.

To prevent abnormal operation caused by low driving voltage and ensure that the chip operates within an appropriate supply voltage range, an undervoltage locking circuit is embedded. The VCC undervoltage high and low values falls into the level trigger category, the VBS undervoltage high value falls into the edge trigger category, the HIN edge retrigger is required, and the VBS undervoltage low value falls into the level trigger type.

Figure 7 VCC Undervoltage Timing Diagram (ignoring transmission delay)

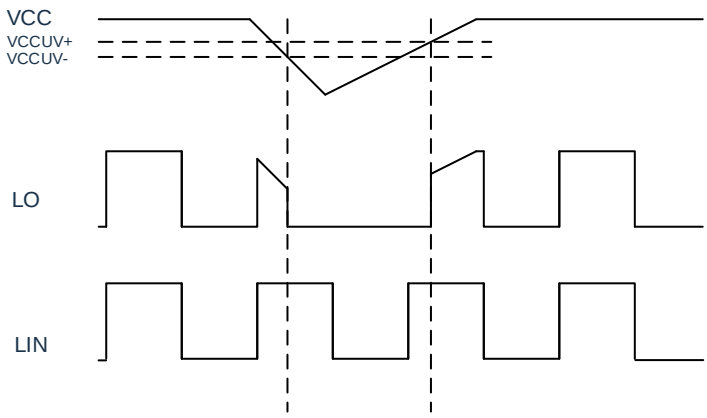
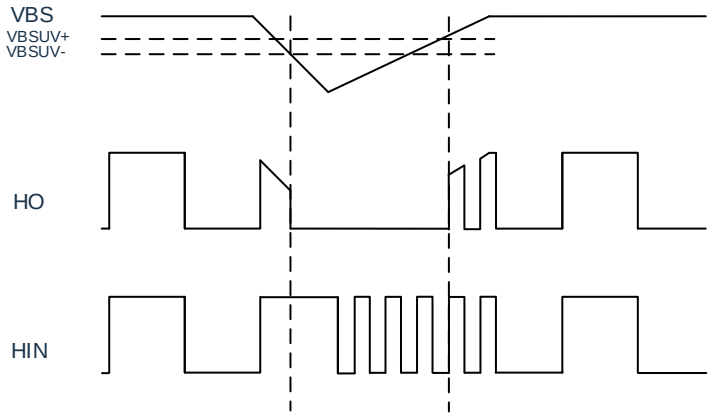


Figure 8 VBS Undervoltage Timing Diagram (ignoring transmission delay)

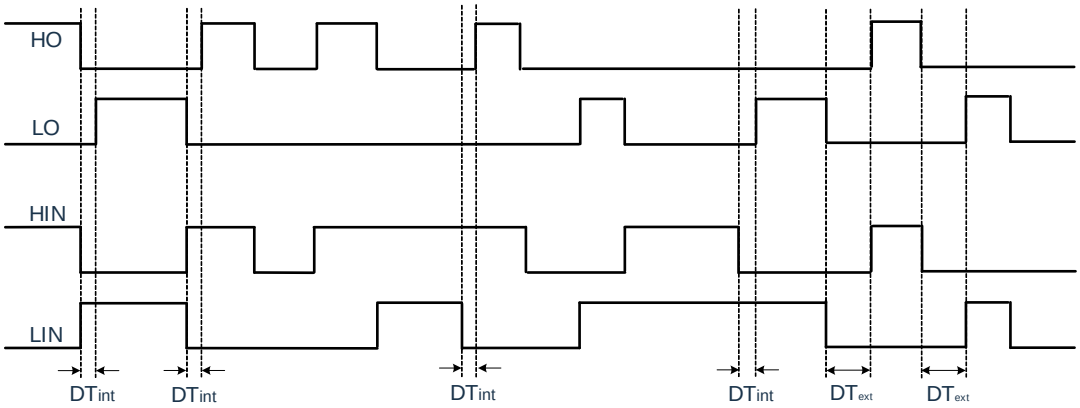


6.3 Straight-through protection and dead time test

A straight-through protection and dead time protection circuit based on the input signal is embedded in the chip. The double high level on the input logic will be determined as a straight-through signal, and the corresponding output will be set to low; moreover, it ensures that at least one dead time is embedded between the output high levels under any input condition. The logic of the external dead time DT_{ext} given on the input end and the embedded dead time DT_{int} is as follows:

- If $T_{ext}>DT_{int}$, $DT=DT_{ext}$
- If $DT_{ext}<DT_{int}$, $DT=DT_{int}$

Figure 9 Logic Timing Diagram (ignoring transmission delay)



7 Package information

7.1 TSSOP20 package diagram

Figure 10 TSSOP20 Package Diagram

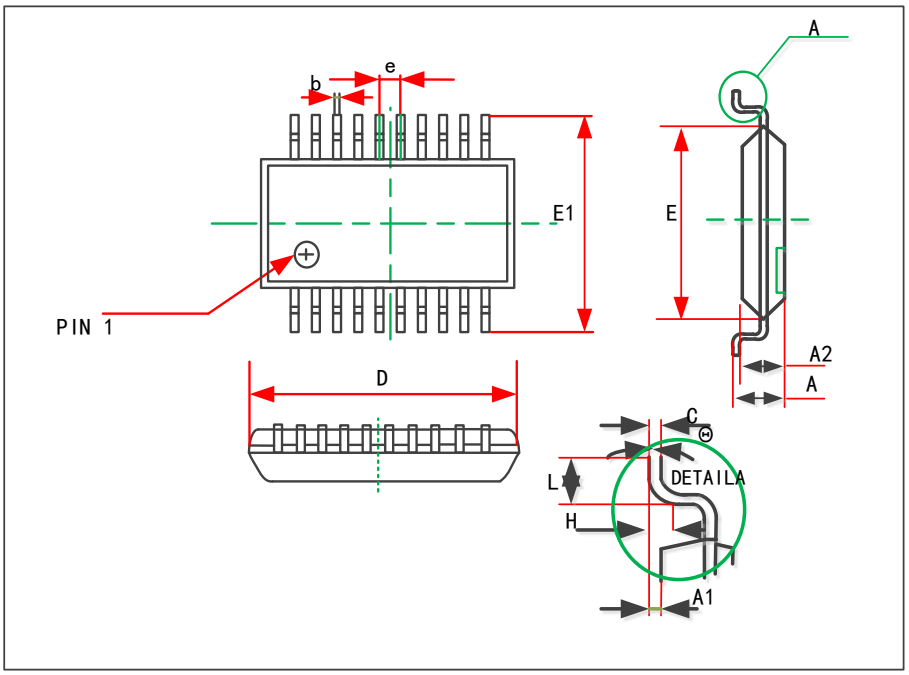


Table 16 TSSOP20 Package Data

SYMBOL	Dimensions IN Millimeters		Dimensions IN Inches	
	MIN	MAX	MIN	MAX
D	6.400	6.600	0.252	0.259
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A	-	1.200	-	0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

Note: (1) Dimensions are marked in millimeters.

(2) BSC is a unit without error, which refers to millimeter here.

Figure 11 TSSOP20 Recommended Welding Layout

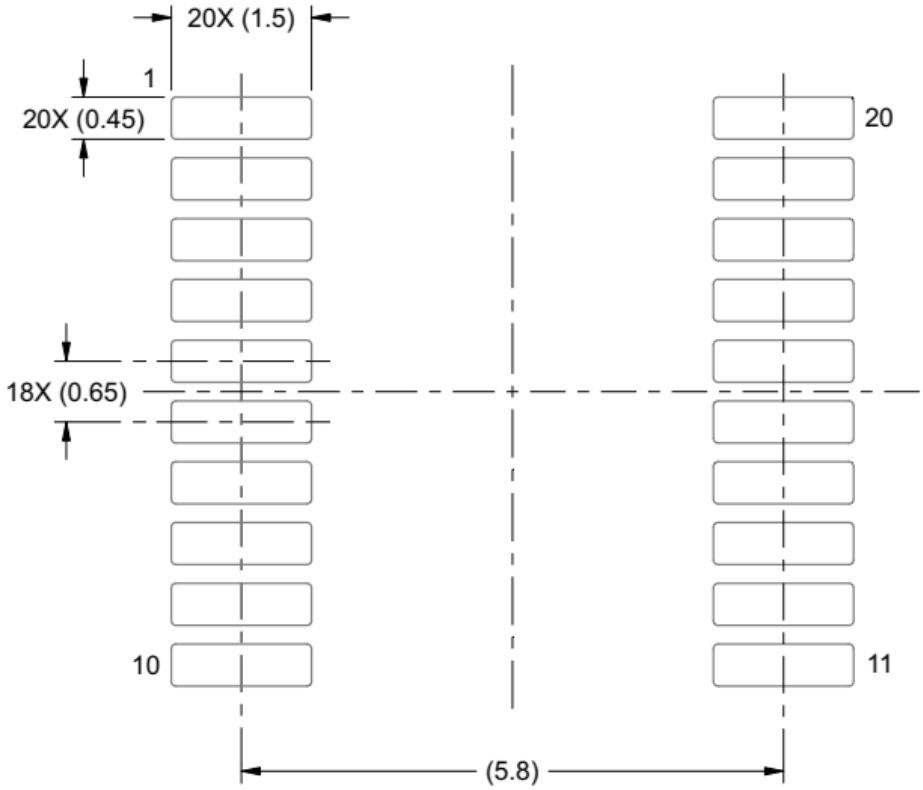
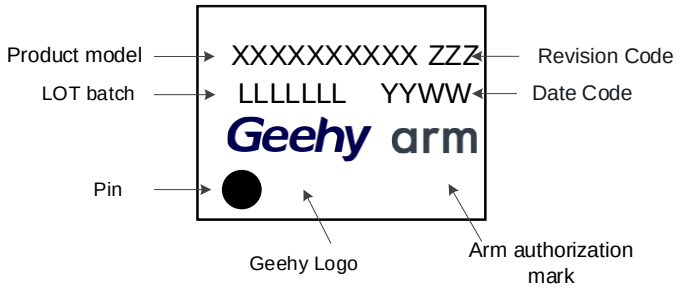
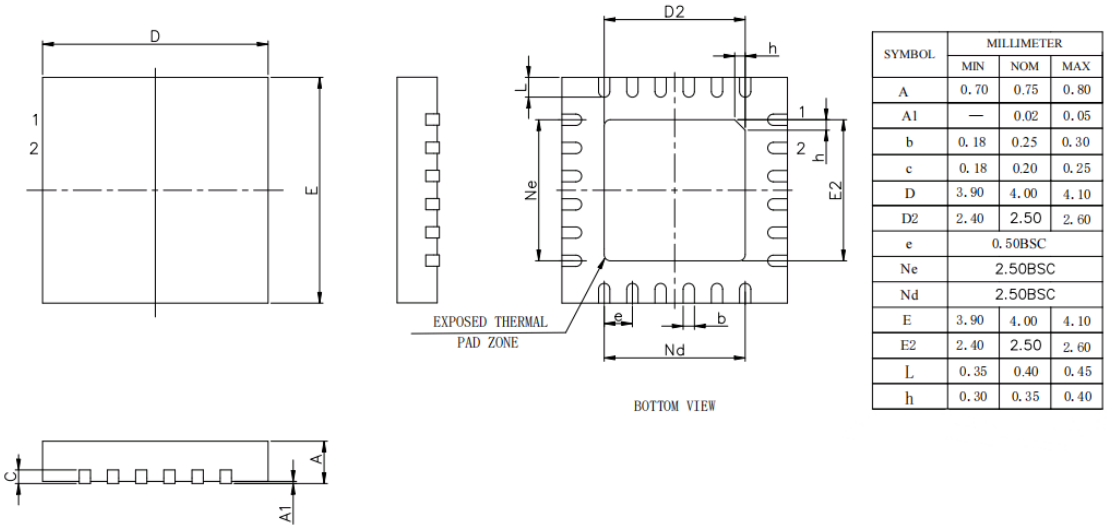


Figure 12 Identification Diagram



7.2 QFN24 package diagram

Figure 13 QFN24 Package Diagram



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.40	2.50	2.60
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.40	2.50	2.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Figure 14 QFN24 Recommended Welding Layout

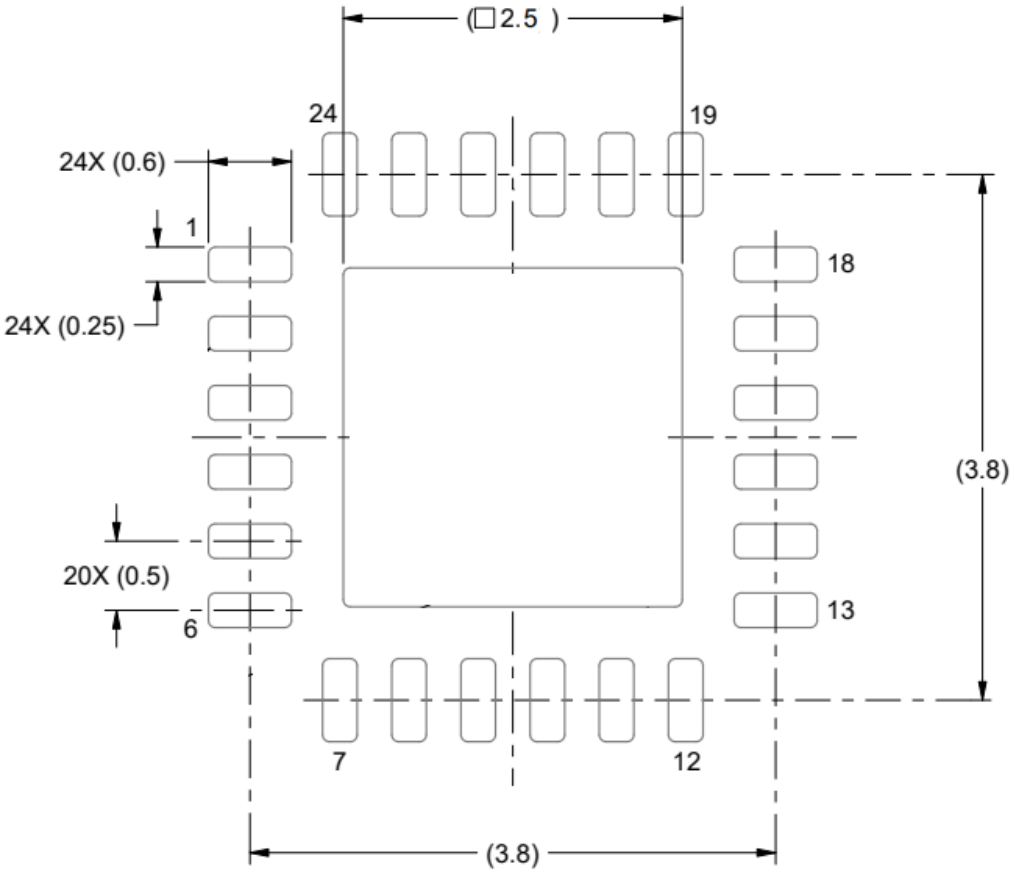
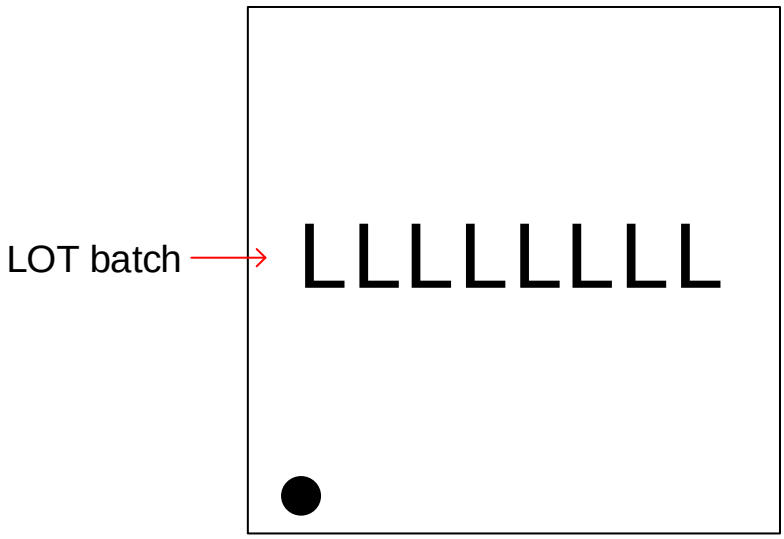


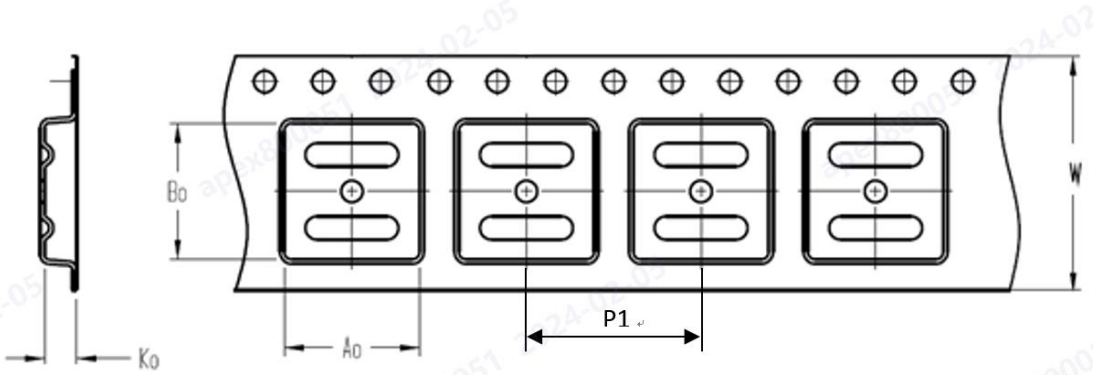
Figure 15 Identification Diagram



8 Packaging Information

8.1 Reel Packaging

Figure 16Tape Dimensions



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
P1	Dimension designed to accommodate the component pitch
W	Overall width of the carrier tape

Figure 17 Quadrant allocation in PIN1 direction in tape

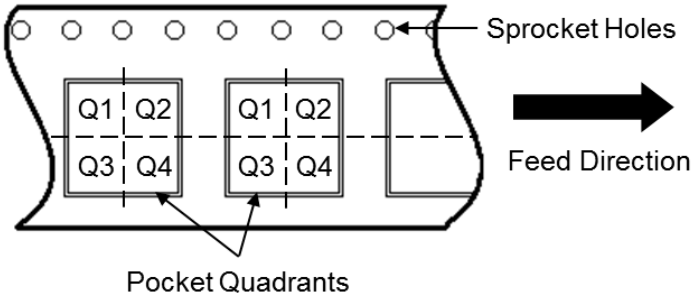


Figure 18 Reel Dimensions

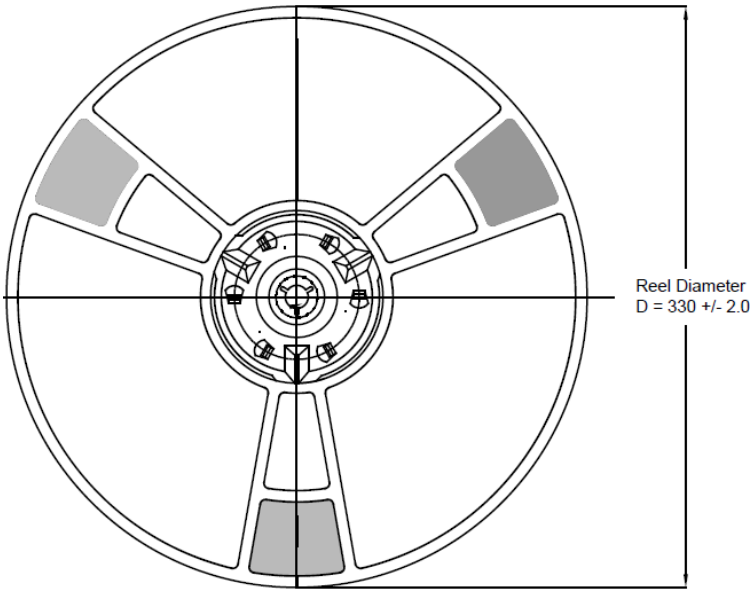
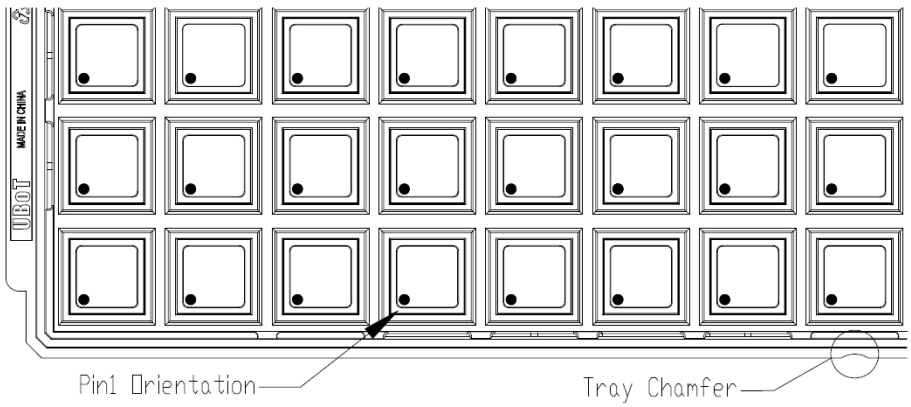


Table 17 Tape packaging parameter specification table

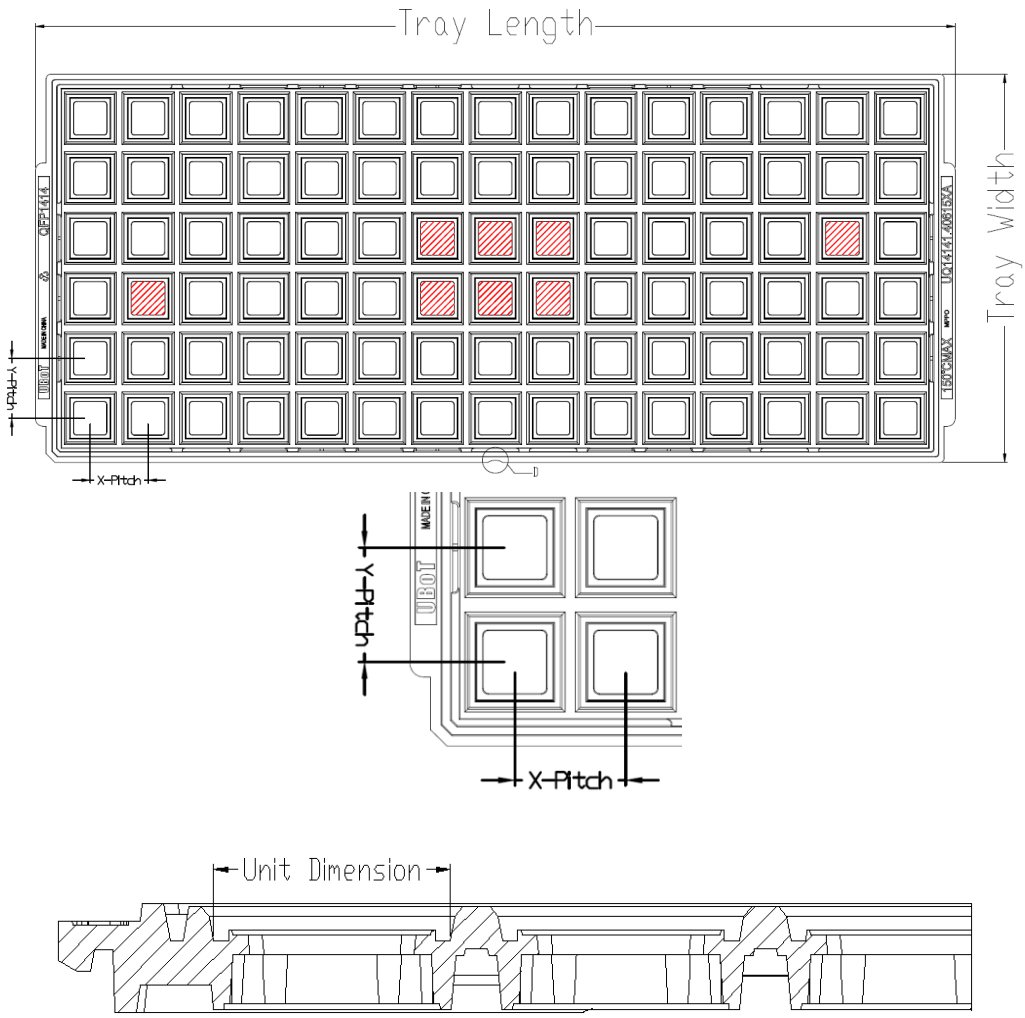
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	P1 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
GHD3440PF	TSSOP	20	9000	330	6.8	6.9	8	1.5	16	Q1

8.2 Tray packaging

Figure 19 Tray Packaging Diagram



Tray Dimensions



All photos are for reference only, and the appearance is subject to the product

Table 18 Tray Packaging Parameter Specification Table

Device	PKG Type	Pins	SPQ	X-Dimension	Y-Dimension	X-Pitch	Y-Pitch	Tray Length	Tray Width
GHD3440QE	QFN	20	4900	4.2	4.2	8.8	9.2	322.6	135.9

9 Ordering information

Table 19 Ordering Information

Product model	Package	Packaging
GHD3440PF	TSSOP20	Reel
GHD3440QE	QFN24	Tray

10 Revision history

Table 20 Document Revision History

Date	Version	Revision History
July 2024	V1.0	New

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